AN11014

BGX7100 evaluation board application note

Rev. 1.0 — 13 April 2012 **Application note**

Document information

Info	Content
Keywords	BGX7100, I/Q modulator, EVB, IP3, CP1, NF, PCB
Abstract	This application note describes the BGX7100 evaluation board (EVB) design and its performance. BGX7100 is an I/Q modulator designed for base station applications. This EVB includes the 50 Ω standard SMA connectors for ease of evaluation.

Revision history

Rev	Date	Description
1.0	20120413	Initial version

Contact information

For more information, please visit: http://www.nxp.com

For sales office addresses, please send an email to: salesaddresses@nxp.com

1. Introduction

The evaluation board (EVB) described in this document allows evaluating the BGX7100.

This document provides the EVB circuit schematic, the bill of materials of the board, the information about PCB technology and its artwork, list of equipments for a typical test set-up required to evaluate the device, and finally the typical test results expected to be obtained.

2. Product Description

The BGX7100 is a high linearity I/Q modulator and provides 1.5 dB of typical voltage gain, 11 dBm of 1 dB output compression point (OCP_{1dB}) and 27 dBm typical outputs $IP3_O$. BGX7100 has 200 Ω differentials I/Q input termination internally. Thanks to its flexible input $V_{i(cm)}$ feature, any common mode voltage value between 0.25 V up to 3.3 V can be acceptable for similar RF performances.

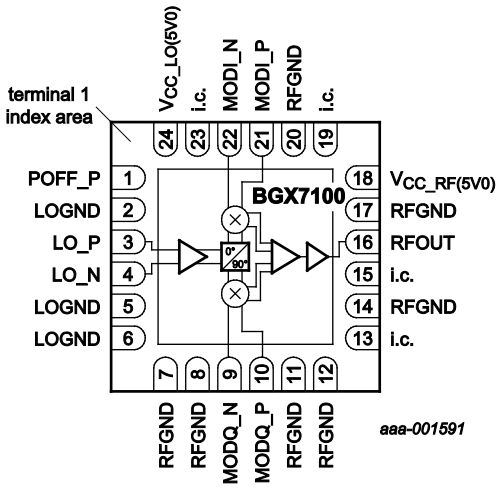


Fig 1. **Pin description**

Its high level of integration enables easy application usage and reduced BOM. Dedicated power OFF/ON pin permits to switch ON or OFF the device. In addition, multiple supply and ground pins allow for independent supply domains to improve the isolation between blocks.

3. EVB Circuit Description

The evaluation board was built on a 25 mil, 4 layers PCB using FR4 based technology and is illustrated in Fig.2 associated with its schematic in Fig.3.

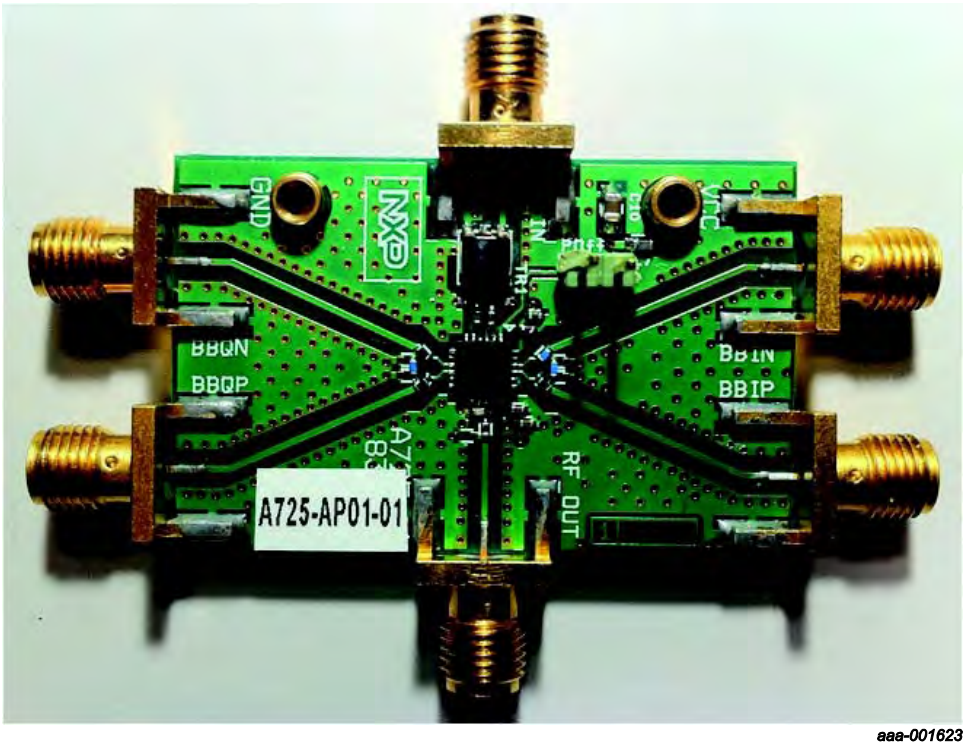


Fig 2. **Evaluation board**

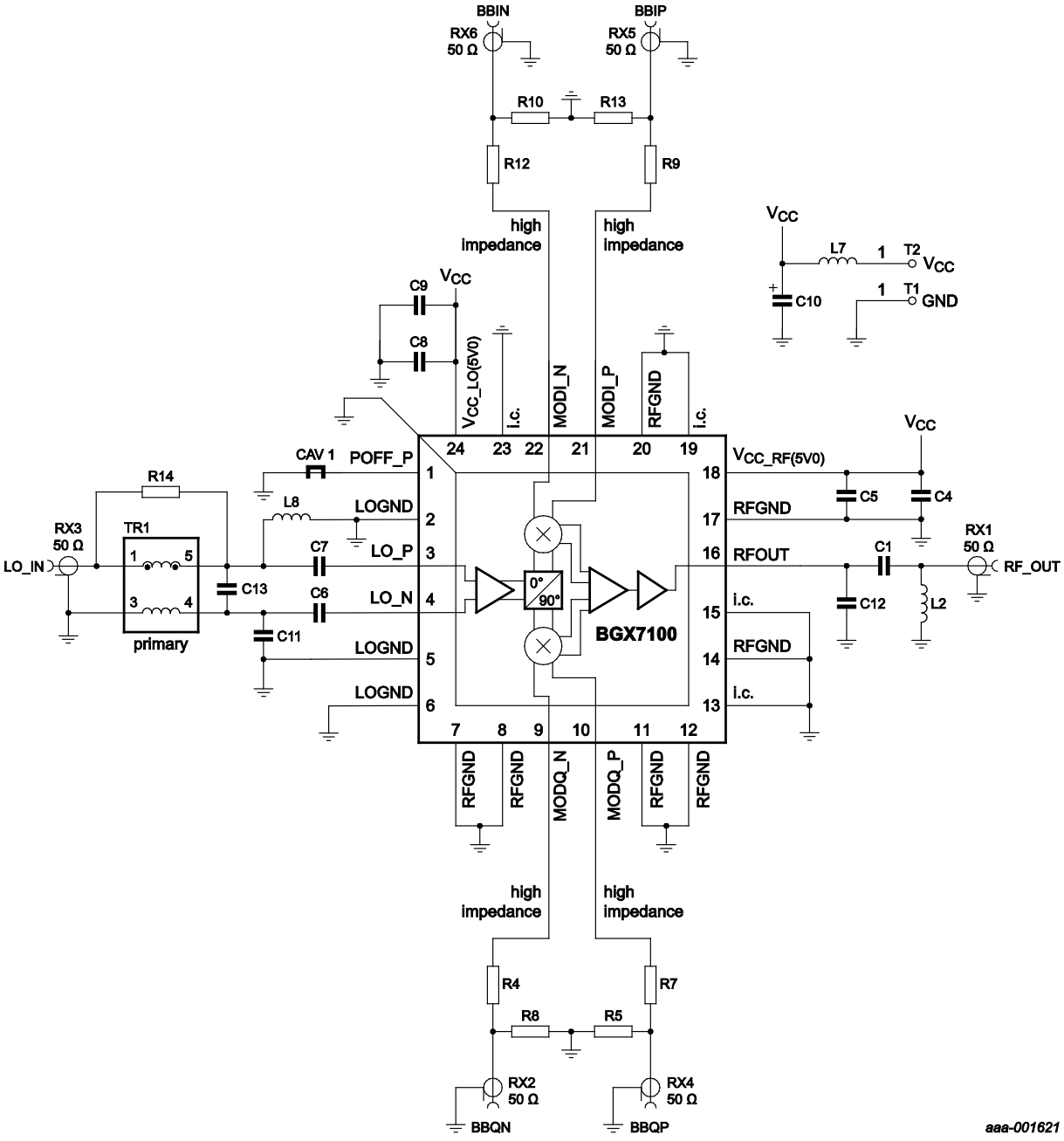


Fig 3. **Evaluation board schematic**

Two LO configuration options available, resulting two bills of material:

1. LO differential (use RF transformer to apply LO in differential between LO_N and LO_P)
2. LO single (LO source connected to LO_P using matching surface mount component, LO_N connected to ground using a DC bypass capacitor)

Choice depends on performances to be achieved.

LO differential mode will be chosen to improve image suppression and IP2. Whereas LO single mode will be chosen to improve LO leakage.

Bill Of Material (BOM) of BGX7100 EVB – LO differential

Reference	Part	Description	Package	Vendors	Qty	Values
T1, T2	2 mm 200 – 52 Banana Plug	supply connector		Multi Contact	2	
RX1, RX2, RX3, RX4, RX5, RX6	142-0701-851	SMA connector, 50 Ω		Emerson/Johnson	6	
L7	BLM18SG700TN1D	ferrite bead	0603	Murata	1	
C10		capacitor	0805	Murata	1	4.7 µF / 16 V
CAV1	2.54 mm header 2 ways	Poff drive		Samtec	1	
C6, C7	COG	capacitor	0402	Murata	2	18 pF
C4, C9	COG	capacitor	0402	Murata	2	100 nF
C1	COG	capacitor	0403	Murata	1	39 pF
C5, C8	COG	capacitor	0402	Murata	2	22 pF
C12	GJM1555C1HR70WB01	capacitor	0402	Murata	1	0.8 pF
C13	GJM1555C1HR30WB01	capacitor	0402	Murata	1	0.3 pF
C11	NC					
L2, L8	NC					
TR1	TC1-1-43A+	LO transformer	AT224 – 1A	Mini-circuits	1	
R4, R7, R9, R12		resistor	0402	Murata	4	0 Ω
R5, R8, R10, R13, R14	NC					
U1	BGX7100	I/Q modulator	HVQFN24 (SOT616 – 3)	NXP	1	

Bill Of Material (BOM) of BGX7100 EVB – LO single

Reference	Part	Description	Package	Vendors	Qty	Values
T1, T2	2 mm 200 – 52 Banana Plug	supply connector		Multi Contact	2	
RX1, RX2, RX3, RX4, RX5, RX6	142-0701-851	SMA connector, 50 Ω		Emerson/Johnson	6	
L7	BLM18SG700TN1D	ferrite bead	0603	Murata	1	
C10		capacitor	0805	Murata	1	4.7 µF / 16 V
CAV1	2.54 mm header 2 ways	Poff drive		Samtec	1	
C7, C11	COG	capacitor	0402	Murata	2	12 pF
C4, C9	COG	capacitor	0402	Murata	2	100 nF
C1	COG	capacitor	0402	Murata	1	39 pF
C5, C8	COG	capacitor	0402	Murata	2	22 pF
C12	GJM1555C1HR70WB01	capacitor	0402	Murata	1	0.8 pF
L2	NC					
L8		inductor	0402	Murata	1	
C13	NC					
TR1	NC					
R4, R7, R9, R12, R14, C6		resistor	0402	Murata	6	0 Ω
R5, R8, R10, R13	NC					
U1	BGX7100	I/Q modulator	HVQFN24 (SOT616 – 3)	NXP	1	

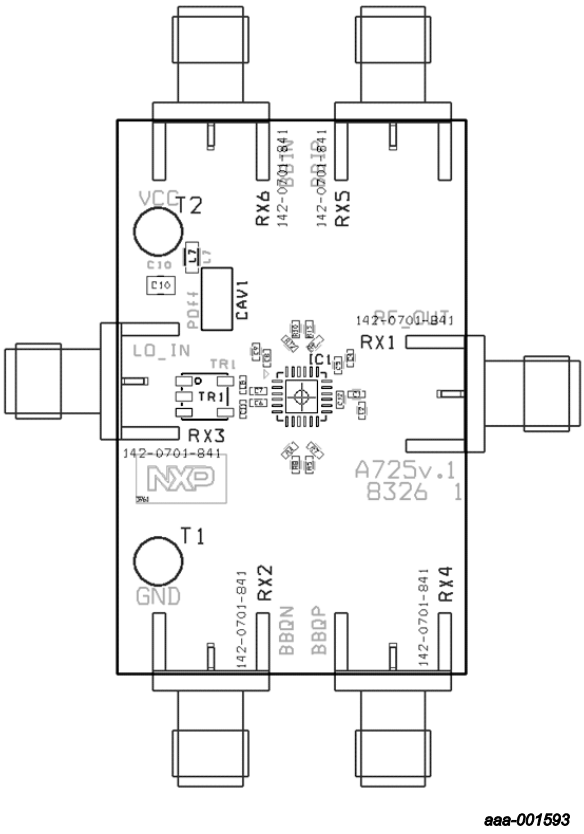


Fig 4. **Evaluation board component placement**

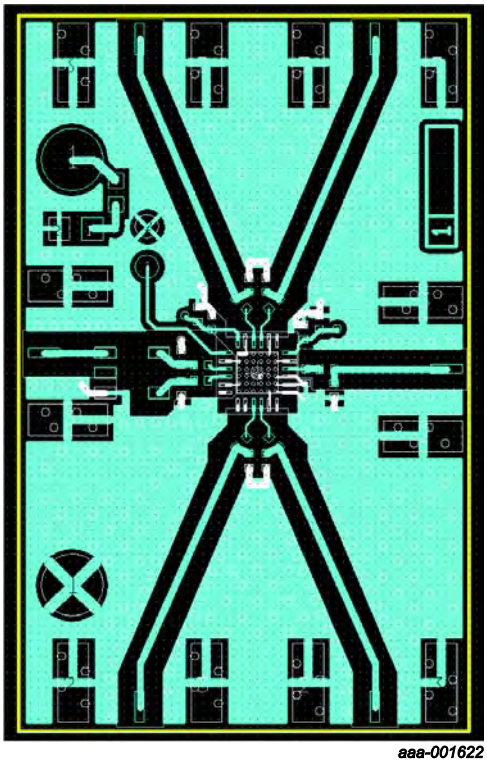


Fig 5. **Evaluation board top layer PCB layout**

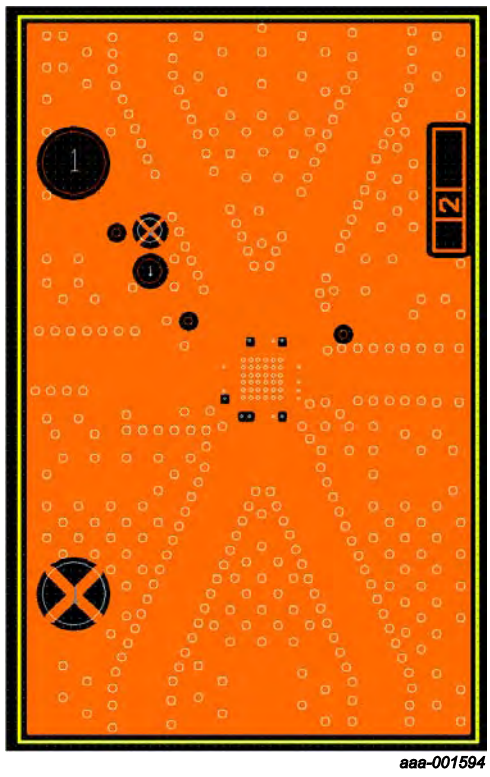


Fig 6. **Evaluation board inner layer_1 PCB layout**

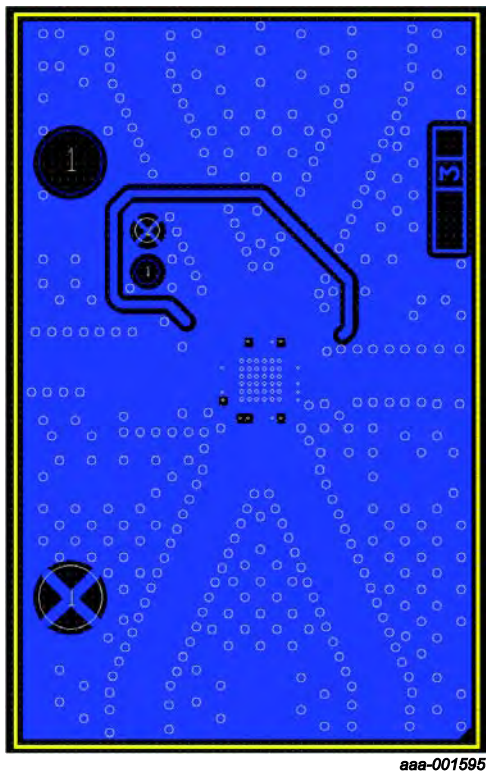


Fig 7. **Evaluation board inner layer_2 PCB layout**

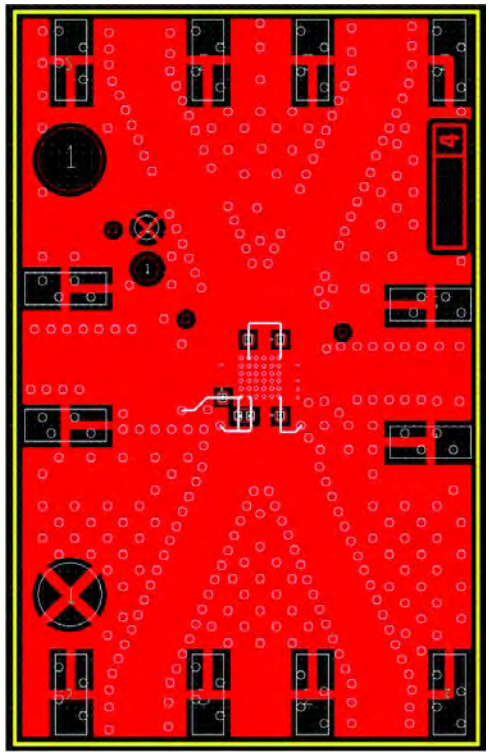
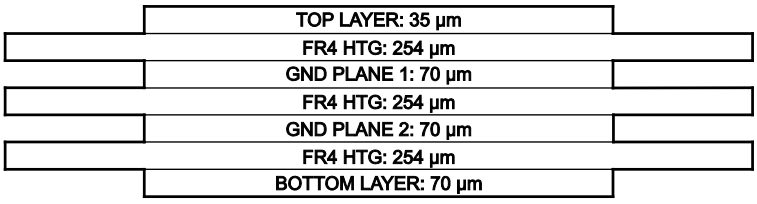


Fig 8. **Evaluation board bottom layer PCB layout**



(1) Etching class: Class5 standard.
(2) Minimum copper conductor with: 150 µm.
(3) Minimum conductor spacing: 150 µm.
(4) Ni-Au (Cobalt) finishing: 3 µm - 25 µm of nickel and 0.1 µm – 1.5 µm of gold.
(5) Board dimension: 45.5 mm x 28.75 mm.
(6) Solder mask both sides green color.
(7) Silkscreen on top layer white color.
(8) Finished thickness: 1 mm +/- 10 %.
(9) Top layer 460 µm traces are controlled impedance, 50 Ω lines.

Fig 9. **Evaluation board PCB technology**

4. Test Setup

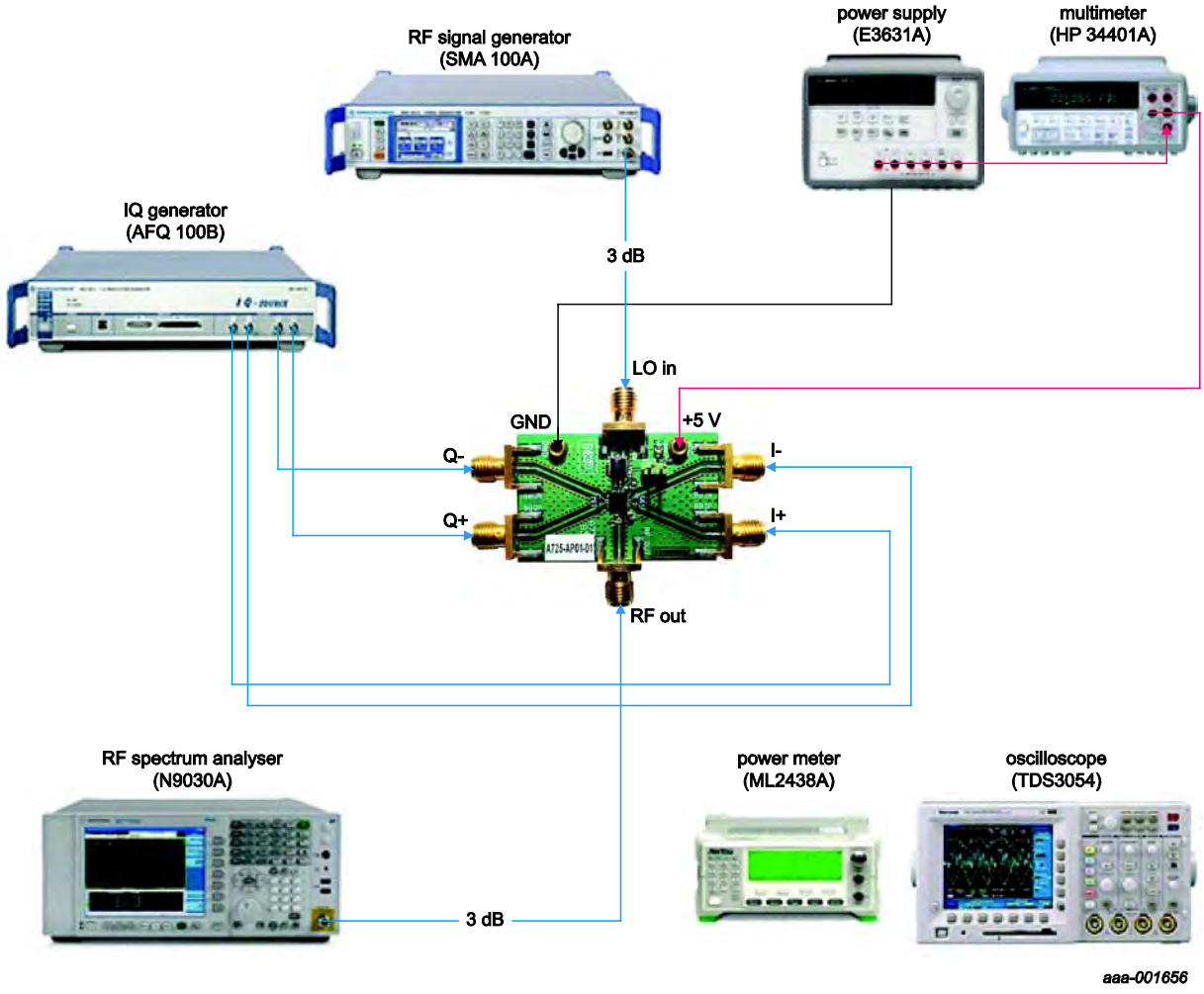


Fig 10. **Test setup block diagram**

5. Quick Start

The BGX7100 EVB kit is fully assembled and factory tested.

Test Equipment Required

Fig 10 shows the equipment required to verify the operation of the BGX7100 EVB kit. It is intended as a guide only, and some substitutions are possible.

Connections

This section provides a step-by-step guide to testing the basic functionality of the EVB kit. As a general precaution to prevent damaging the outputs by driving high-VSWR loads, **do not turn on DC power or RF signal generators until all connections are made:**

1. Connect 3 dB pads to the DUT ends of each RF signal generators and SMA cables (RF OUT / LO IN). This padding improves VSWR, and reduces the errors due to mismatch.
2. Measure loss in 3 dB pads and cables. Use this loss as an offset in all output power/gain calculations.
3. Disable all RF signal sources.
4. Connect the signal sources to the appropriate SMA inputs.
5. Set the LO and IF signal generators according to the following:
   - IF AWG signal source: 1 V (p-p) differential into DUT at 5 MHz
   - LO signal source: 0 dBm into DUT at 1960 MHz

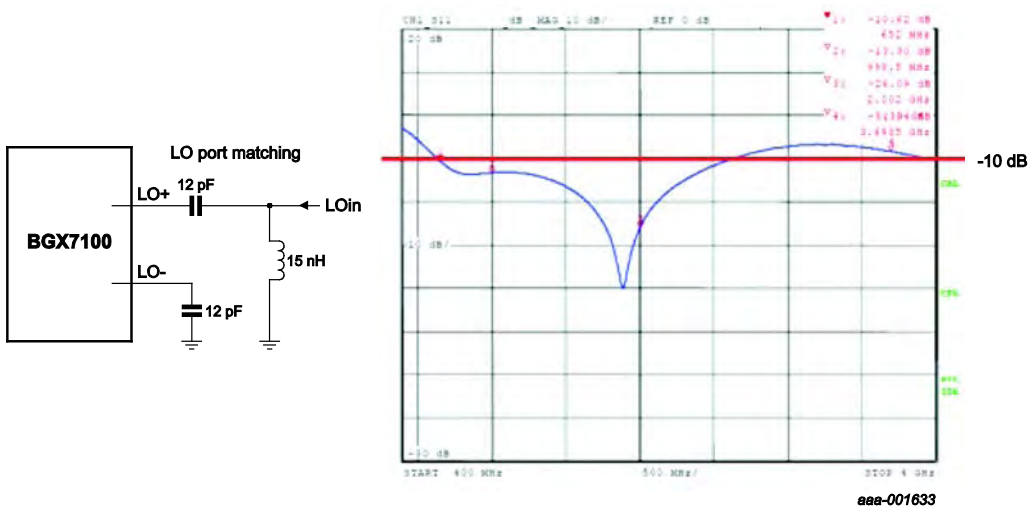
   (f_{RF} = 1965 MHz)
6. Set the DC supply to +5.0 V and set a current limit around 250 mA. Connect supplies to the EVB kit through the ammeter. Turn on the supply.

   Readjust the supply to get +5.0 V at the EVB kit. There will be a voltage drop across the ammeter when the mixer is drawing current.
7. Enable the LO and the IF sources.

6. Typical Operating Characteristics

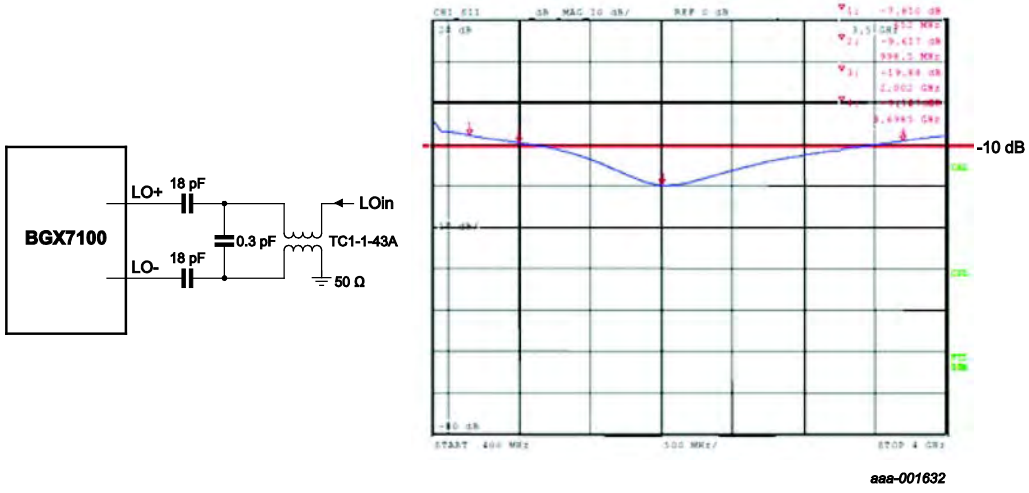
6.1 RF measurements:

V_{CC} = 5 V, P_{RF} = - 10 dBm, $P_{i(lo)}$ = 0 dBm, T_C = +25 °C.



(1) Matching optimized for 2 GHz frequency range.

Fig 11. **LO port input matching single ended**



(1) Matching optimized for 2 GHz frequency range.

Fig 12. **LO port input matching differential**

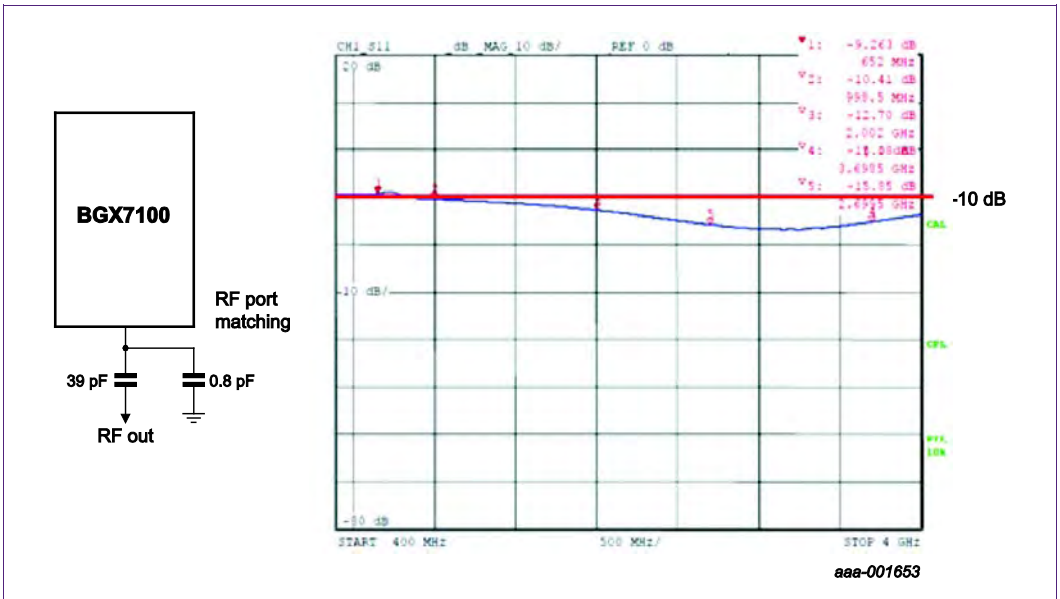


Fig 13. **RF port output matching**

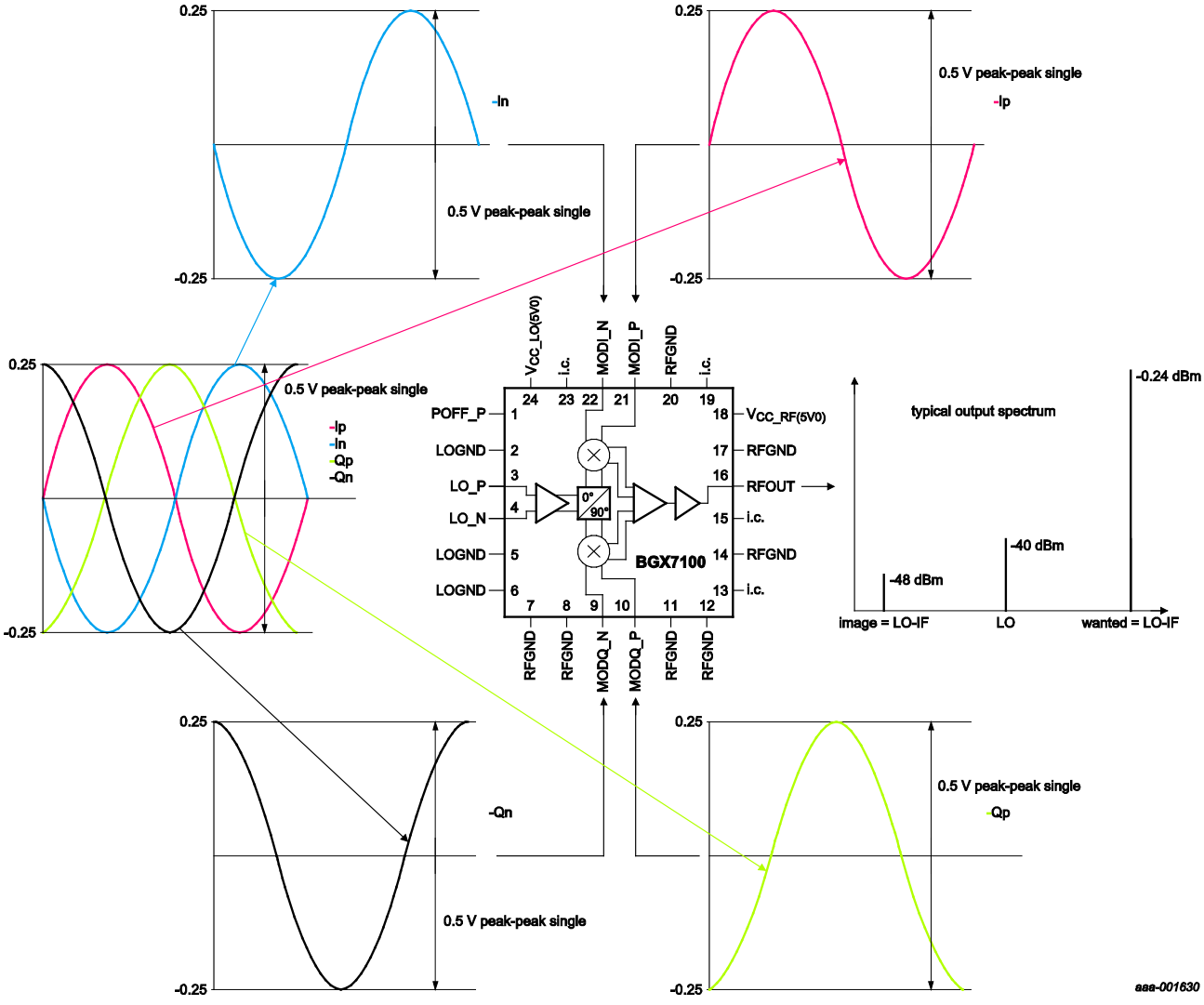
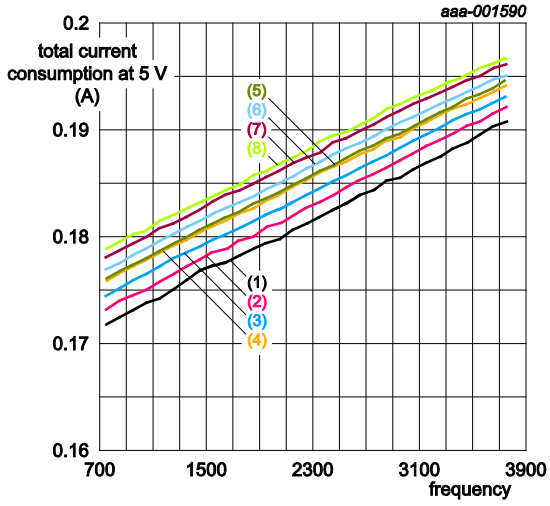
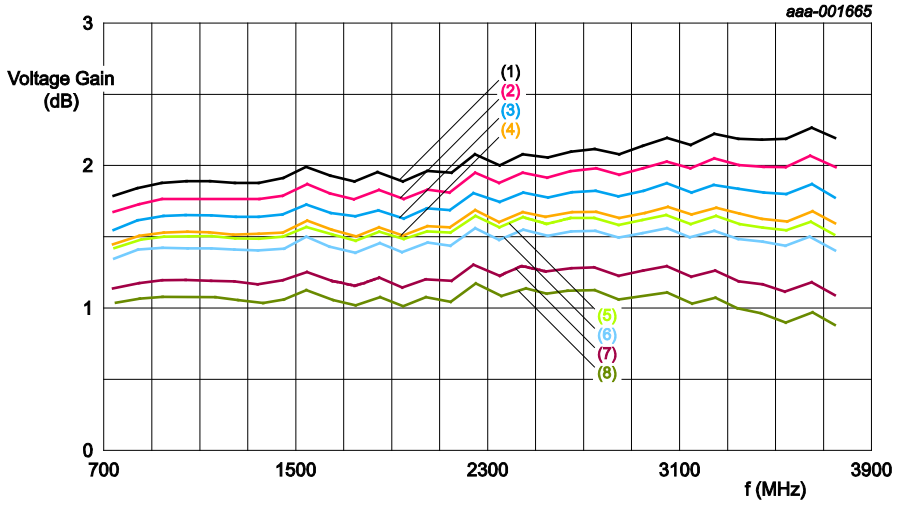


Fig 14. **I/Q input signal**



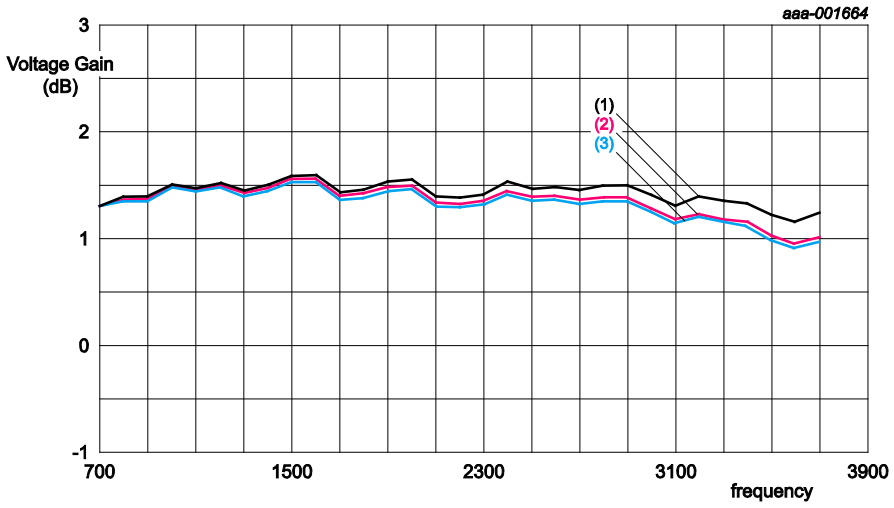
(1) Temperature = -40 °C.
(2) Temperature = -20 °C.
(3) Temperature = 0 °C.
(4) Temperature = 20 °C.
(5) Temperature = 25 °C.
(6) Temperature = 40 °C.
(7) Temperature = 60 °C.
(8) Temperature = 80 °C.

Fig 15. **Current consumption**



(1) Temperature = -40 °C.
(2) Temperature = -20 °C.
(3) Temperature = 0 °C.
(4) Temperature = 20 °C.
(5) Temperature = 25 °C.
(6) Temperature = 40 °C.
(7) Temperature = 60 °C.
(8) Temperature = 80 °C.

Fig 16. **Voltage gain versus temperature**



(1) $V_{i(cm)}$ I/Q = 0.5 V.

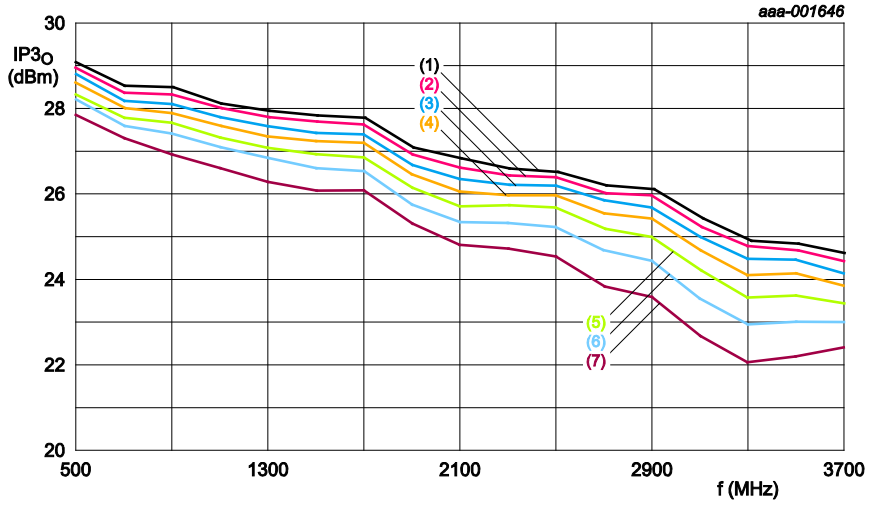
(2) $V_{i(cm)}$ I/Q = 1.7 V.

(3) $V_{i(cm)}$ I/Q = 2.5 V.

Small dependency with input common mode voltage on I/Q inputs.

Power level collected with a spectrum analyzer, which explains the variations.

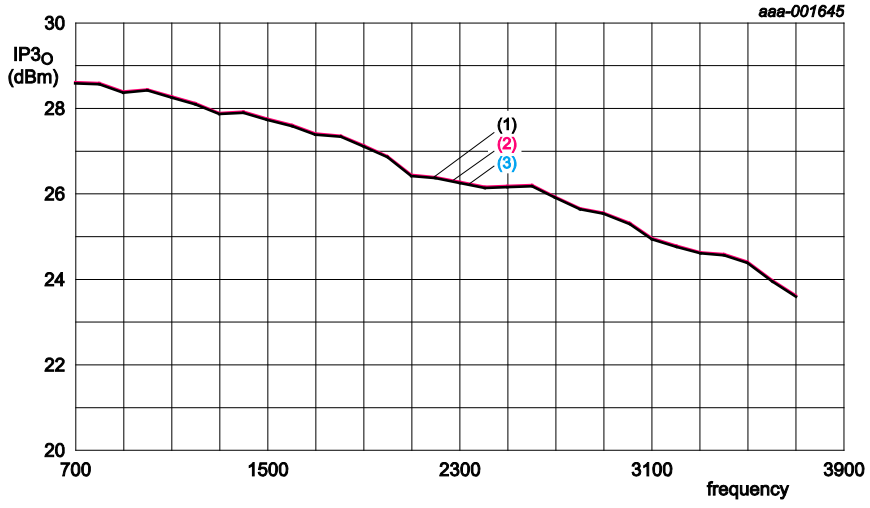
Fig 17. **Voltage gain versus common mode**



(1) Temperature = -40 °C.
(2) Temperature = -20 °C.
(3) Temperature = 0 °C.
(4) Temperature = 20 °C.
(5) Temperature = 40 °C.
(6) Temperature = 60 °C.
(7) Temperature = 80 °C.

I/Q = 5 MHz +/- 0.5 MHz.

Fig 18. **Output $IP3_O$ versus temperature**



(1) $V_{i(cm)}$ = 0.5 V.

(2) $V_{i(cm)}$ = 1.7 V.

(3) $V_{i(cm)}$ = 2.5V.

$IP3_O$ identical for different $V_{i(cm)}$ voltages.

Improved compared to last design.

I/Q = 5 MHz +/- 0.5 MHz.

Fig 19. **Output $IP3_O$ versus common mode**

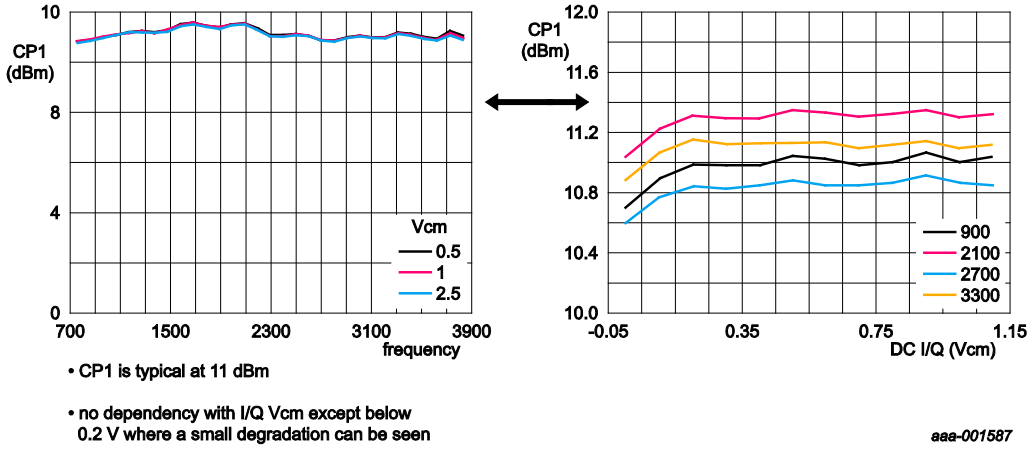
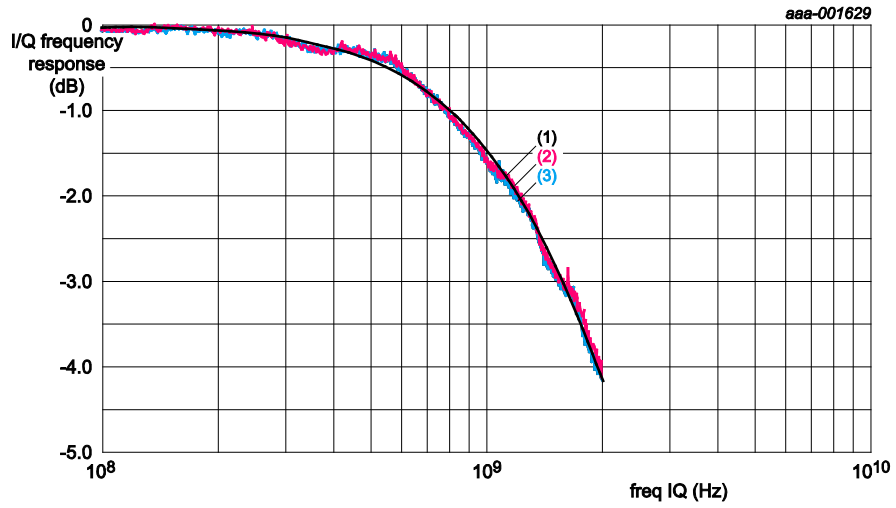


Fig 20. **1 dB compression point**



(1) Q path.

(2) I path.

(3) First order model.

RF generator on each I/Q baseband lines is used so that we can reach high frequencies.

This explains some ups and downs on the attenuation curves.

I/Q lines are well matched.

Estimated first order cut-off frequency around 800 MHz.

Fig 21. **I/Q frequency response**

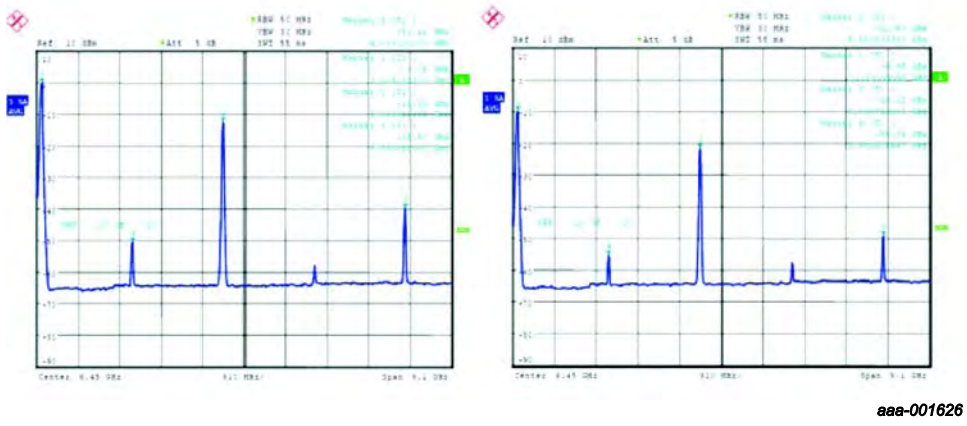
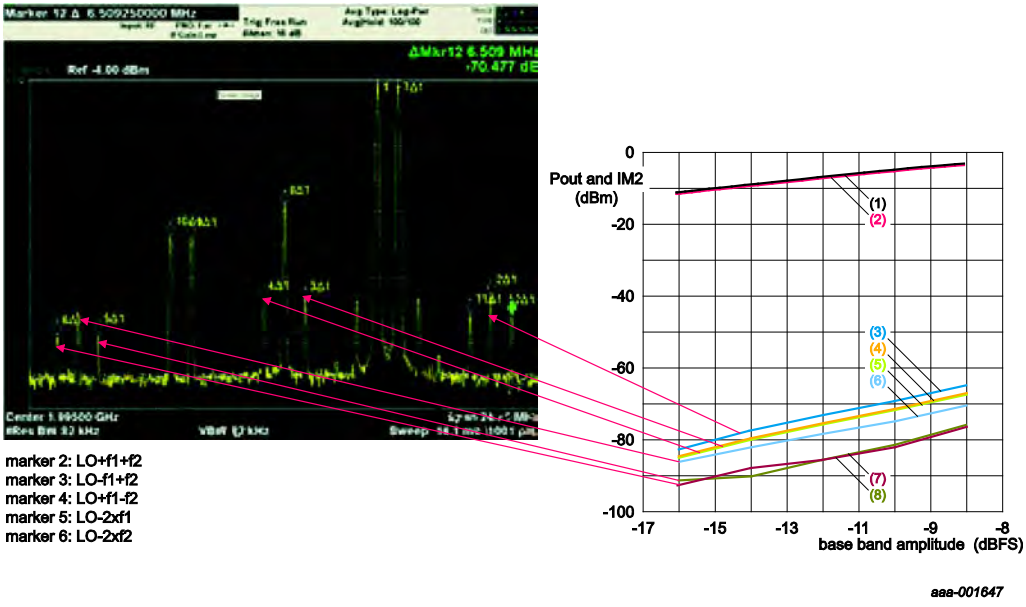


Fig 22. **Harmonic emissions – one tone at 2 GHz**



(1) F1 level (dBm) = -2000 – 6.2.

(2) F2 level (dBm) = -2000 – 6.2.

(3) LO + F1 + F2 level (dBm) = -2000 – 6.2.

(4) LO – (F2 – F1 level (dBm) = -2000 – 6.2.

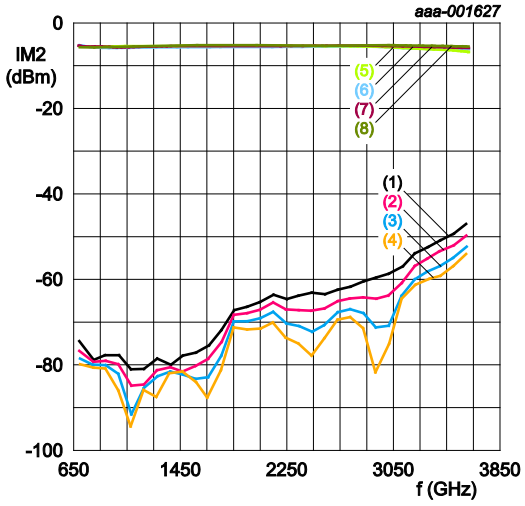
(5) LO – (F1 – F2 level (dBm) = -2000 – 6.2.

(6) LO – F1 – F2 level (dBm) = -2000 – 6.2.

(7) LO – 2F2 level (dBm) = -2000 – 6.2.

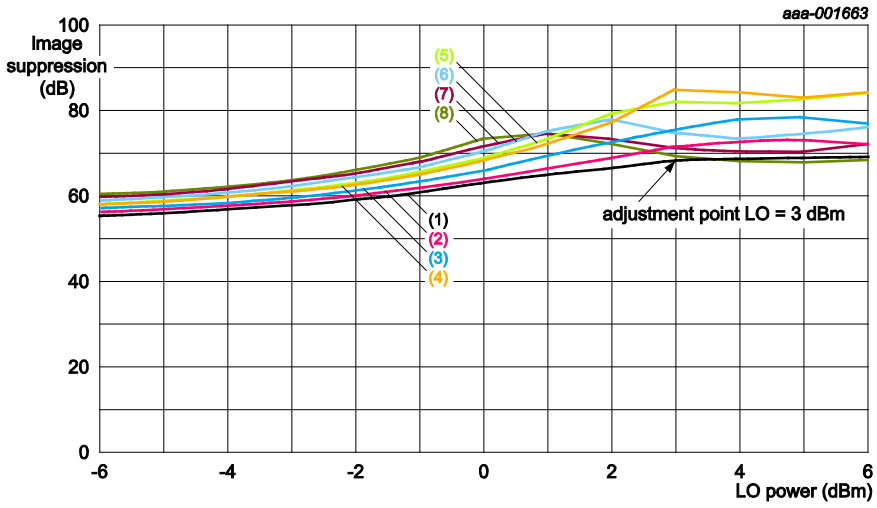
(8) LO – 2F1 level (dBm) = -2000 – 6.2.

Fig 23. **P_o and IM2 at 2 GHz**



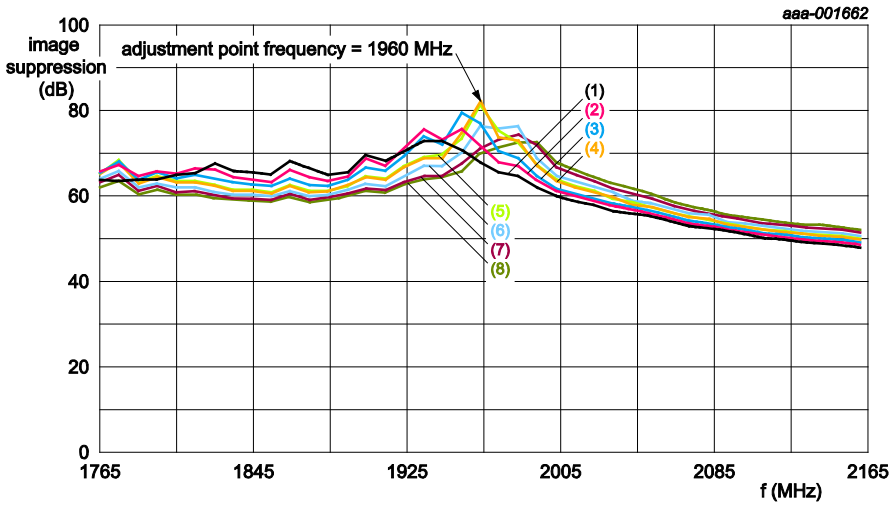
(1) LO + F1 + F2 level (dBm) -0.2 - -10.
(2) LO + F1 + F2 level (dBm) -3.2 - -10.
(3) LO + F1 + F2 level (dBm) -6.2 - -10.
(4) LO + F1 + F2 level (dBm) -9.2 - -10.
(5) F1 level (dBm) -0.2 - -10.
(6) F1 level (dBm) -3.2 - -10.
(7) F1 level (dBm) -6.2 - -10.
(8) F1 level (dBm) -9.2 - -10.

Fig 24. **IM2 versus $P_{i(lo)}$ on all frequency band**



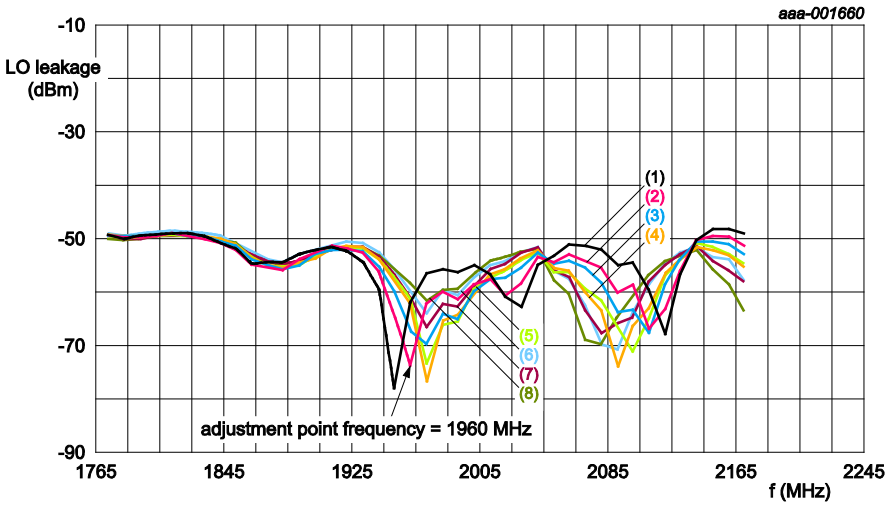
(1) Temperature = -40 °C.
(2) Temperature = -20 °C.
(3) Temperature = 0 °C.
(4) Temperature = 20 °C.
(5) Temperature = 25 °C.
(6) Temperature = 40 °C.
(7) Temperature = 60 °C.
(8) Temperature = 80 °C.

Fig 25. **Unadjusted sideband suppression versus $P_{i(lo)}$ and temperature**



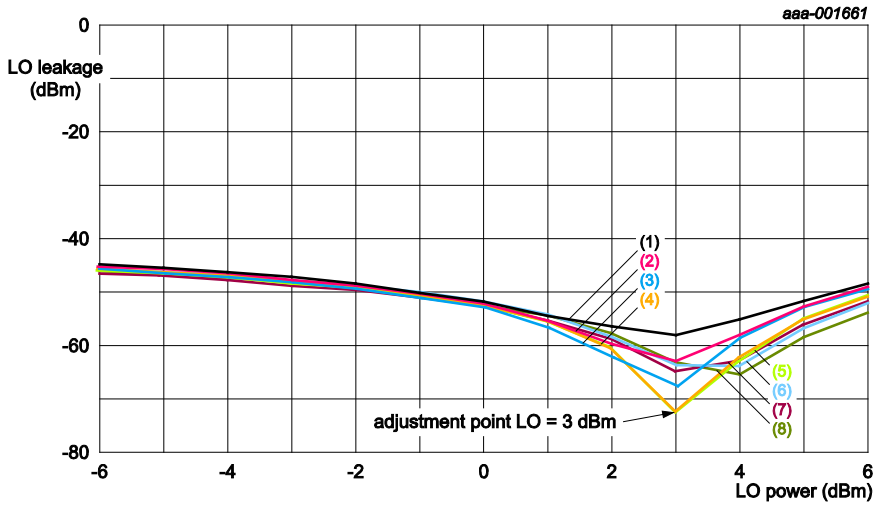
(1) Temperature = -40 °C.
(2) Temperature = -20 °C.
(3) Temperature = 0 °C.
(4) Temperature = 20 °C.
(5) Temperature = 25 °C.
(6) Temperature = 40 °C.
(7) Temperature = 60 °C.
(8) Temperature = 80 °C.

Fig 26. **Unadjusted sideband suppression versus frequency and temperature**



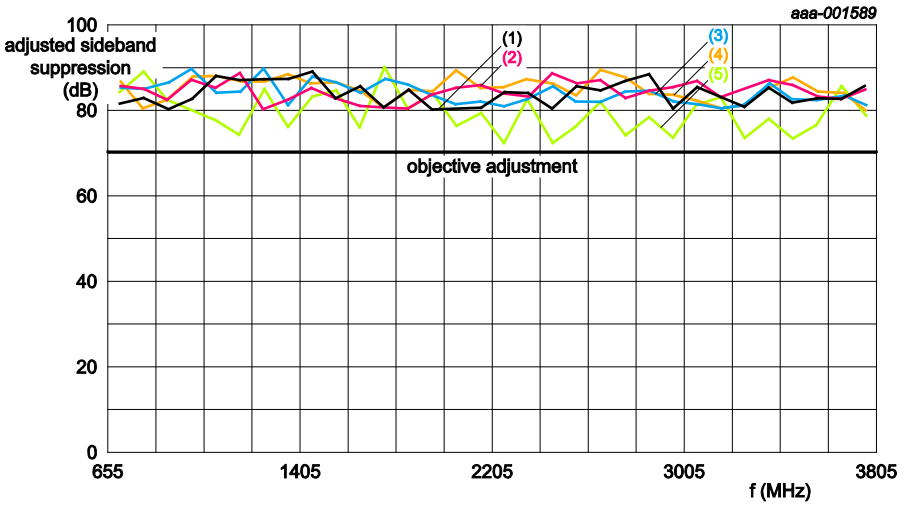
(1) Temperature = -40 °C.
(2) Temperature = -20 °C.
(3) Temperature = 0 °C.
(4) Temperature = 20 °C.
(5) Temperature = 25 °C.
(6) Temperature = 40 °C.
(7) Temperature = 60 °C.
(8) Temperature = 80 °C.

Fig 27. **Unadjusted carrier suppression versus frequency and temperature**



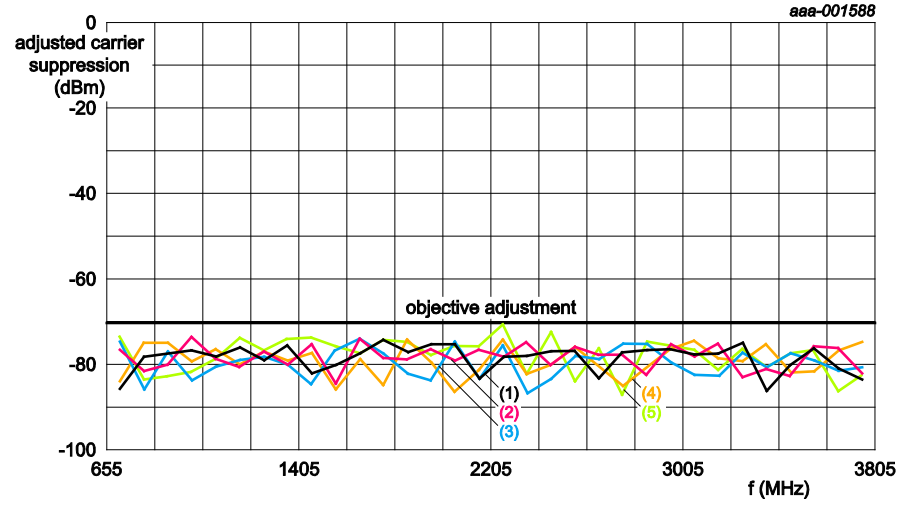
(1) Temperature = -40 °C.
(2) Temperature = -20 °C.
(3) Temperature = 0 °C.
(4) Temperature = 20 °C.
(5) Temperature = 25 °C.
(6) Temperature = 40 °C.
(7) Temperature = 60 °C.
(1) Temperature = 80 °C.

Fig 28. **Unadjusted carrier suppression versus $P_{i(lo)}$ and temperature**



(1) Device number = 5.
(2) Device number = 15.
(3) Device number = 70.
(4) Device number = 75.
(5) Device number = 69.

Fig 29. **Adjusted sideband suppression**



(1) Device number = 5.
(2) Device number = 15.
(3) Device number = 70.
(4) Device number = 75.
(5) Device number = 69.

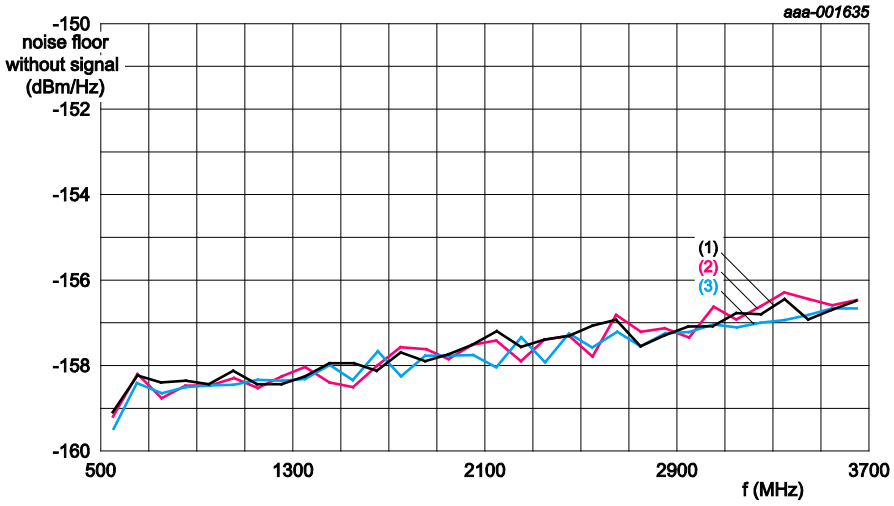
Fig 30. **Adjusted carrier suppression**

DC offset, phase and gain unbalance and on different devices after adjustment

Frequency (MHz)	2000						
Device	Optimal I/Q mismatch phase (deg)	Optimal I/Q mismatch gain (dB)	Optimal I/Q mismatch DC I (mV)	Optimal I/Q mismatch DC Q (mV)	Carrier level (dBm)	Image suppression (dB)	Tx output power (dBm)
5	2.684	-0.229	-2	-0.9	-75.1	80.6	-1.1
15	0.269	-0.013	-4.5	-1.6	-79.1	85.3	-1
70	0.892	-0.005	-4.4	-1.3	-74.1	81.4	-1
75	-0.146	0.007	-4.2	-2.5	-86.3	89.1	-1
69	0.343	-0.008	-2.9	-1.6	-74.4	76.2	-1

DC offset, phase and gain unbalance at different frequency for the same device

Device	69						
Frequency (MHz)	Optimal I/Q mismatch phase (Deg)	Optimal I/Q mismatch gain (dB)	Optimal I/Q mismatch DC I (mV)	Optimal I/Q mismatch DC Q (mV)	Carrier level (dBm)	Image suppression (dB)	Tx output power (dBm)
900	-0.36	0.004	-0.3	-0.7	-81.9	79.6	-1.1
1000	-0.27	0.004	-0.4	-0.9	-78.4	77.5	-1
1800	0.608	-0.003	-2.3	-1.6	-74.8	80.2	-1.2
1900	0.513	-0.007	-2.5	-1.6	-77.8	84.6	-1.1
2000	0.343	-0.008	-2.9	-1.6	-75.4	76.2	-1
2600	-0.15	-0.021	-3.7	-1.9	-76	81.8	-1
3300	-0.377	-0.02	-3.7	-4	-80.7	78	-1.2

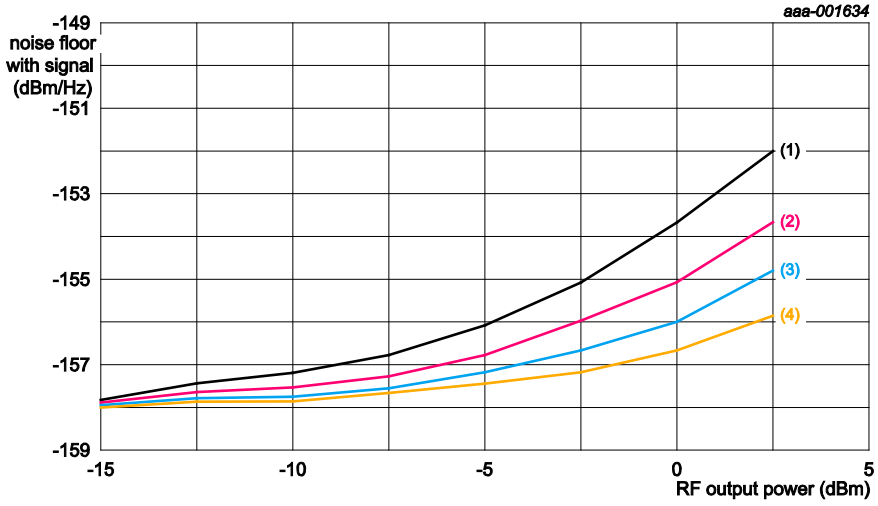


(1) Device number = 15.

(2) Device number = 75.

(3) Device number = 69.

Fig 31. **Noise floor without signal – offset = 5 MHz**



(1) LO power = -3 dBm.

(2) LO power = 0 dBm.

(3) LO power = 3 dBm.

(4) LO power = 6 dBm.

Fig 32. **Noise floor with signal – frequency = 1960 MHz - offset = 10 MHz**

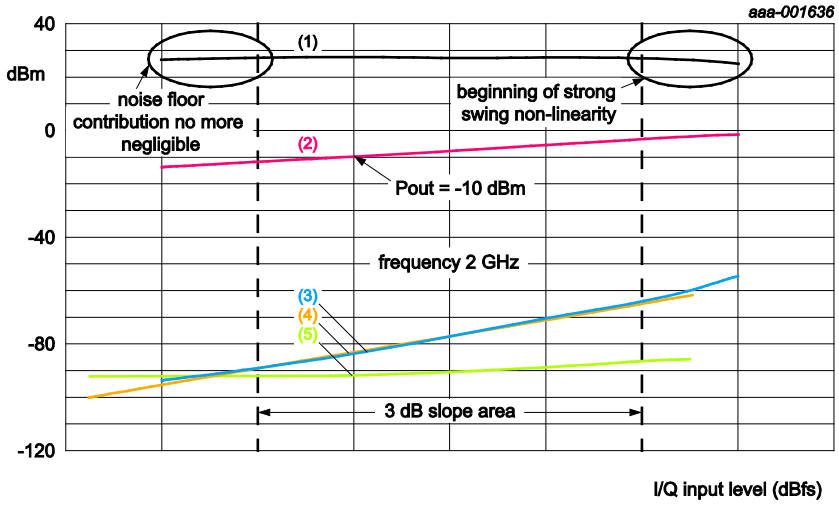
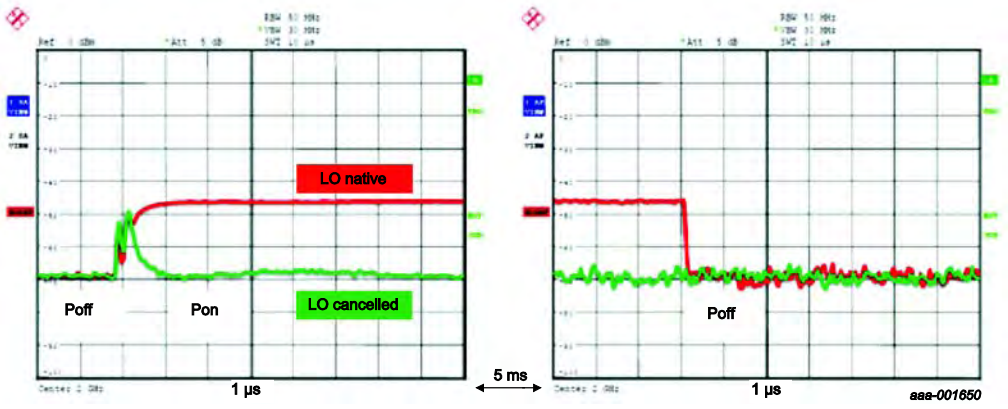
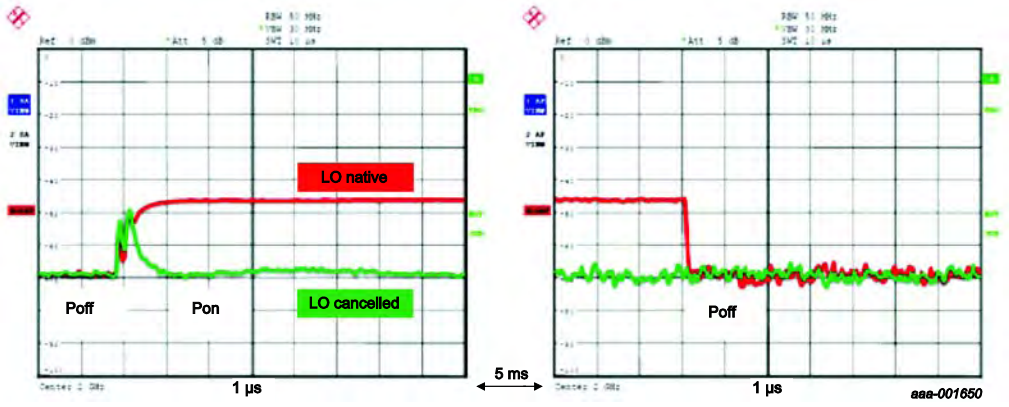


Fig 33. **$IP3_O$, IM3, noise floor and output power**



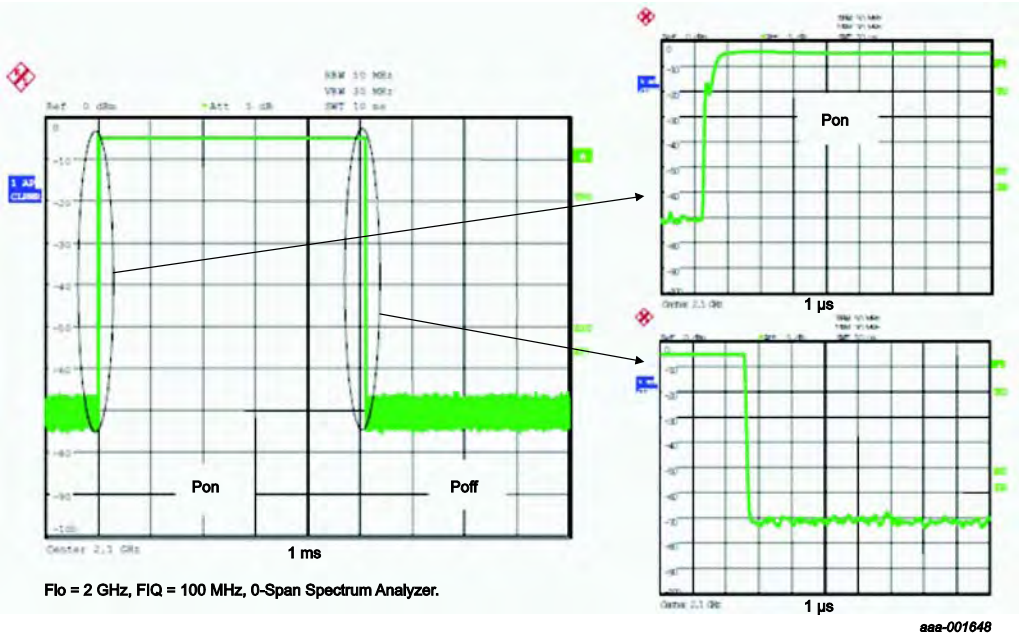
Flo = 2 GHz, 0-Span Spectrum Analyzer.

Fig 34. **Power OFF functionality**



Flo = 2 GHz, 0-Span Spectrum Analyzer.

Fig 35. **Power OFF functionality**

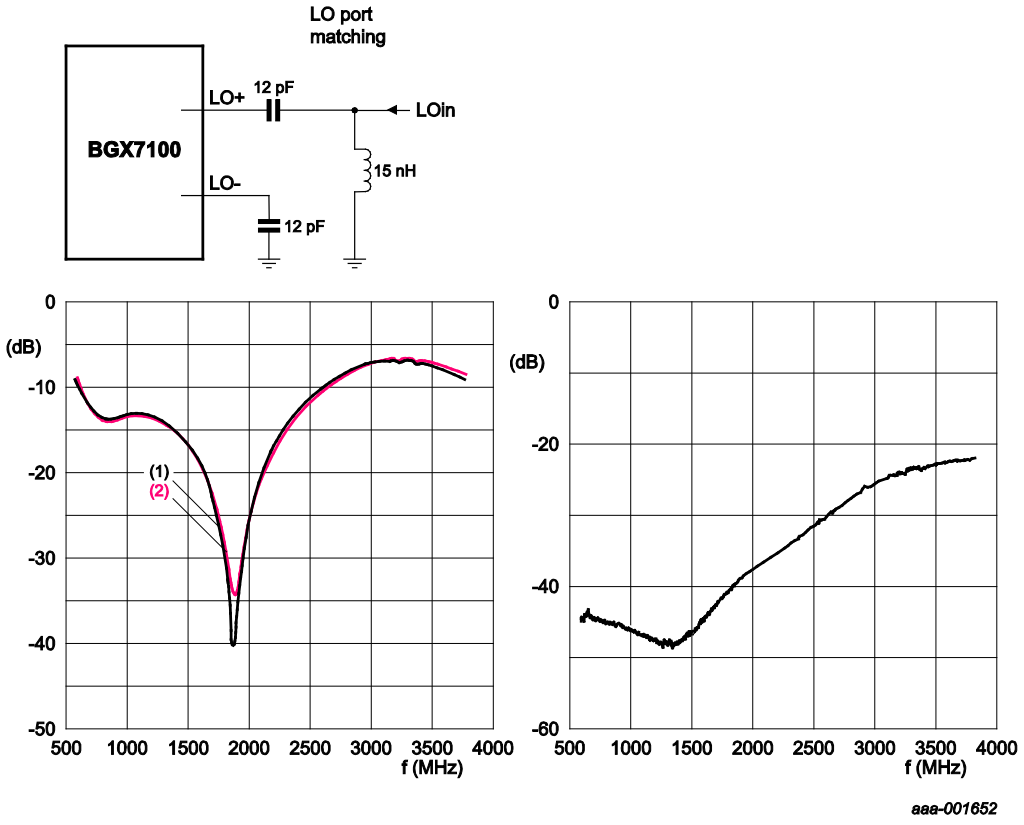


Flo = 2 GHz, FIQ = 100 MHz, 0-Span Spectrum Analyzer.

Fig 36. **Power OFF functionality**

The device could be used in a frequency band extension down to 400 MHz and up to 4 GHz with small degradation on sideband suppression.

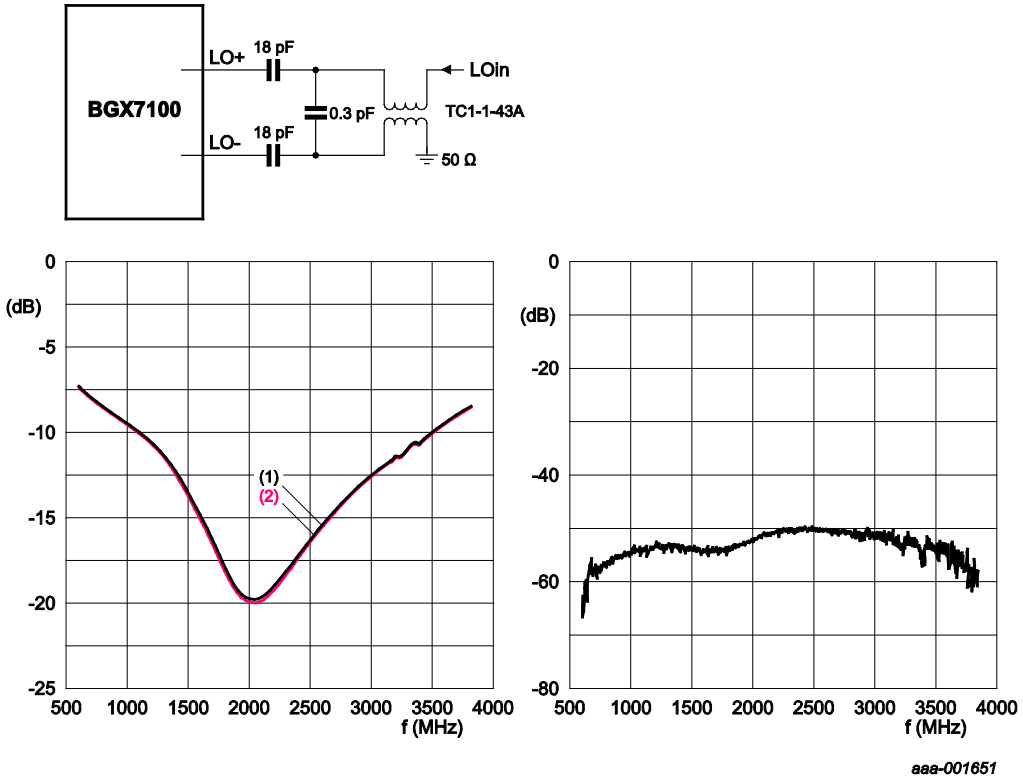
6.2 Comparison between differential and single ended LO input:



(1) dB(S11): POFF_P = shutdown disabled.

(2) dB(S11): POFF_P = shutdown enabled.

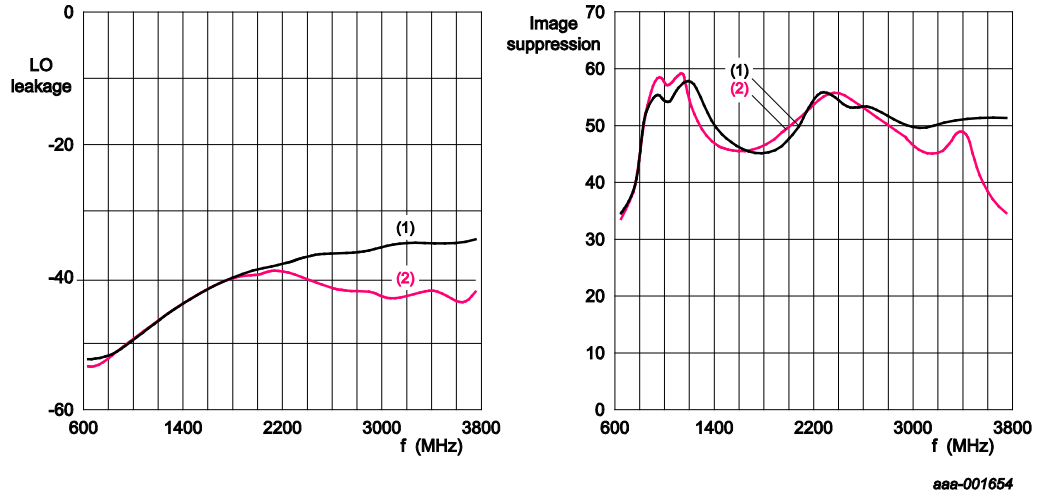
Fig 37. **Power OFF/ON behavior single ended LO port input matching**



(1) dB(S11): POFF_P = shutdown disabled.

(2) dB(S11): POFF_P = shutdown enabled.

Fig 38. **Power OFF/ON behavior differential LO port input matching**

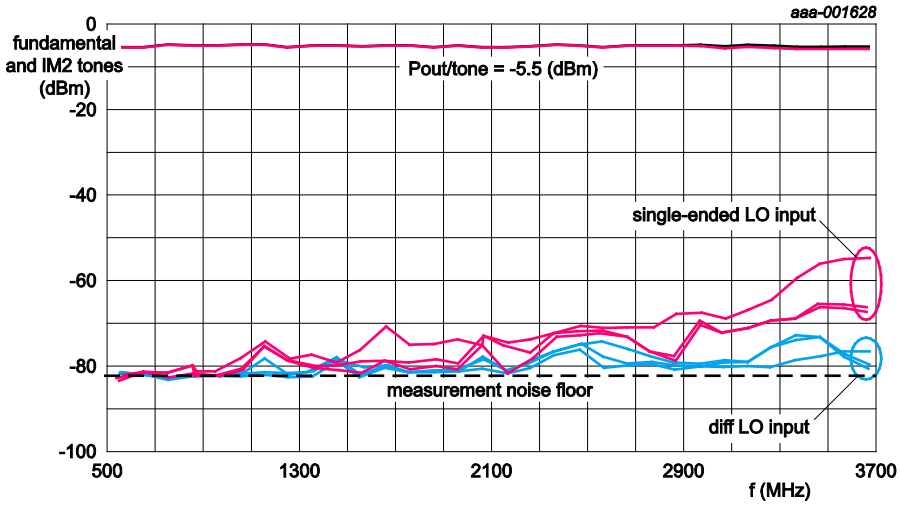


(1) Differential LO input.

(2) Single ended LO input.

Main difference seen at high frequency: differential input is better for Image Rejection but worse for LO Leakage.

Fig 39. **Sideband and carrier suppression versus single ended and differential LO input matching**



3 IM2 products measured: LO + F1 + F2; LO – F1 – F2; LO + F2 – F1.

Differential LO input gives significantly less IM2 power (especially at high frequency).

Fig 40. **IM2 versus single ended and differential LO input matching**

6.3 System measurement:

6.3.1 One carrier GMSK

Fig 41. **One carrier GMSK P_o = 0dBm**

Fig 42. **One carrier GMSK P_o = -5dBm**

6.3.2 One carrier Edge

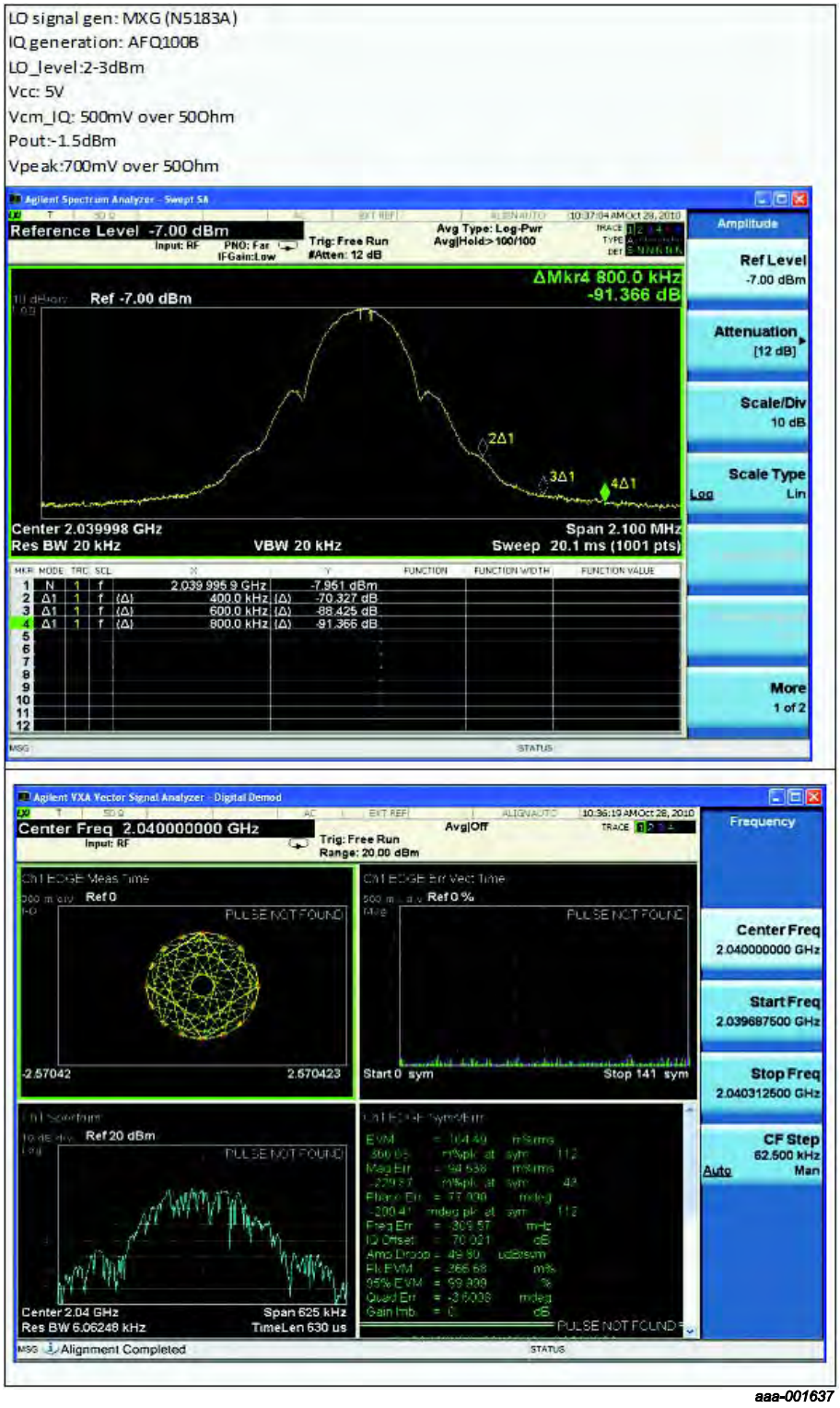
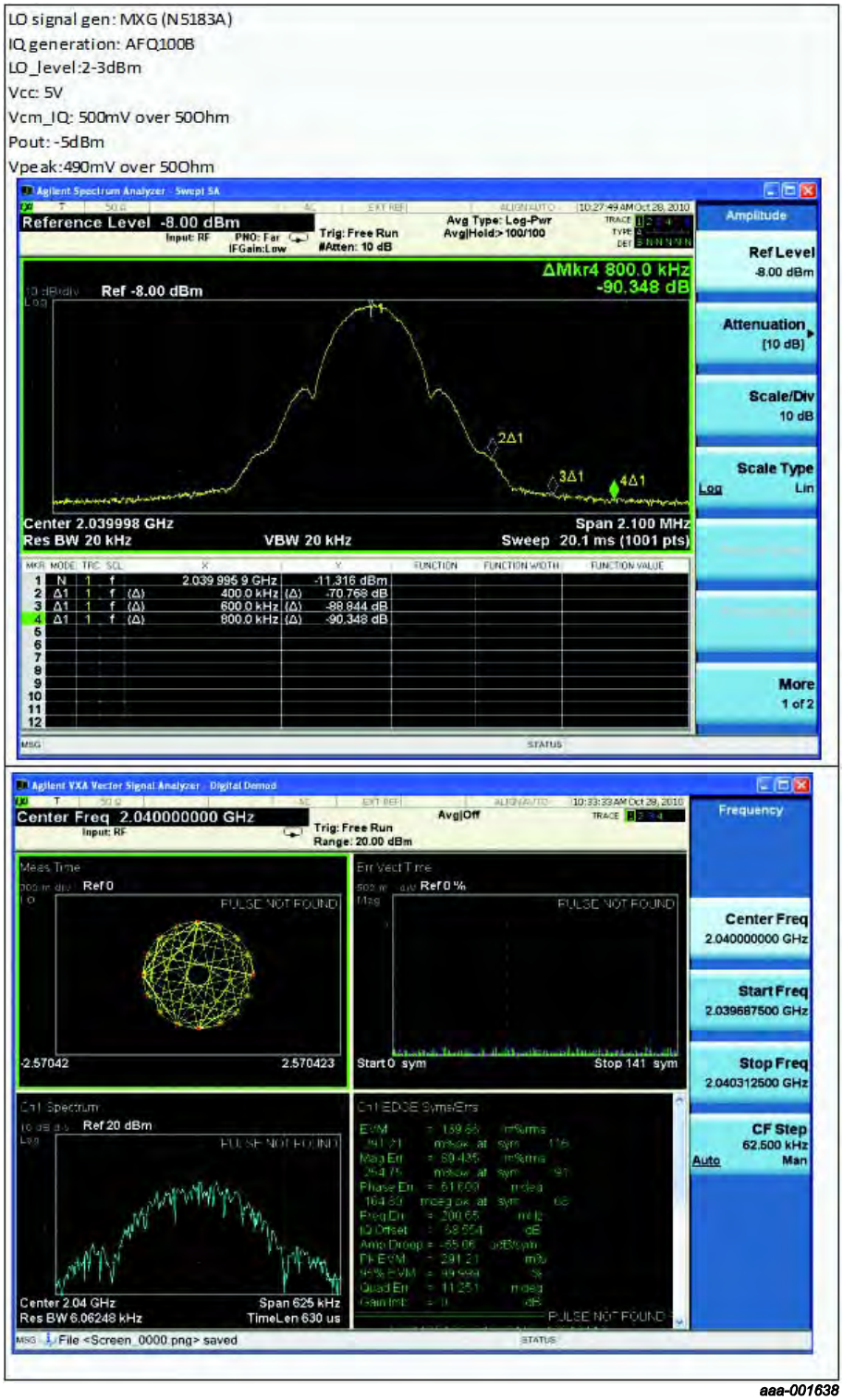


Fig 43. **One carrier EDGE P_o = -1.5dBm**



aaa-001638

Fig 44. **One carrier EDGE P_o = -5dBm**

6.3.3 Six carriers GMSK

Fig 45. **Six carrier GMSK P_o = -10dBm**

6.3.4 One carrier WCDMA

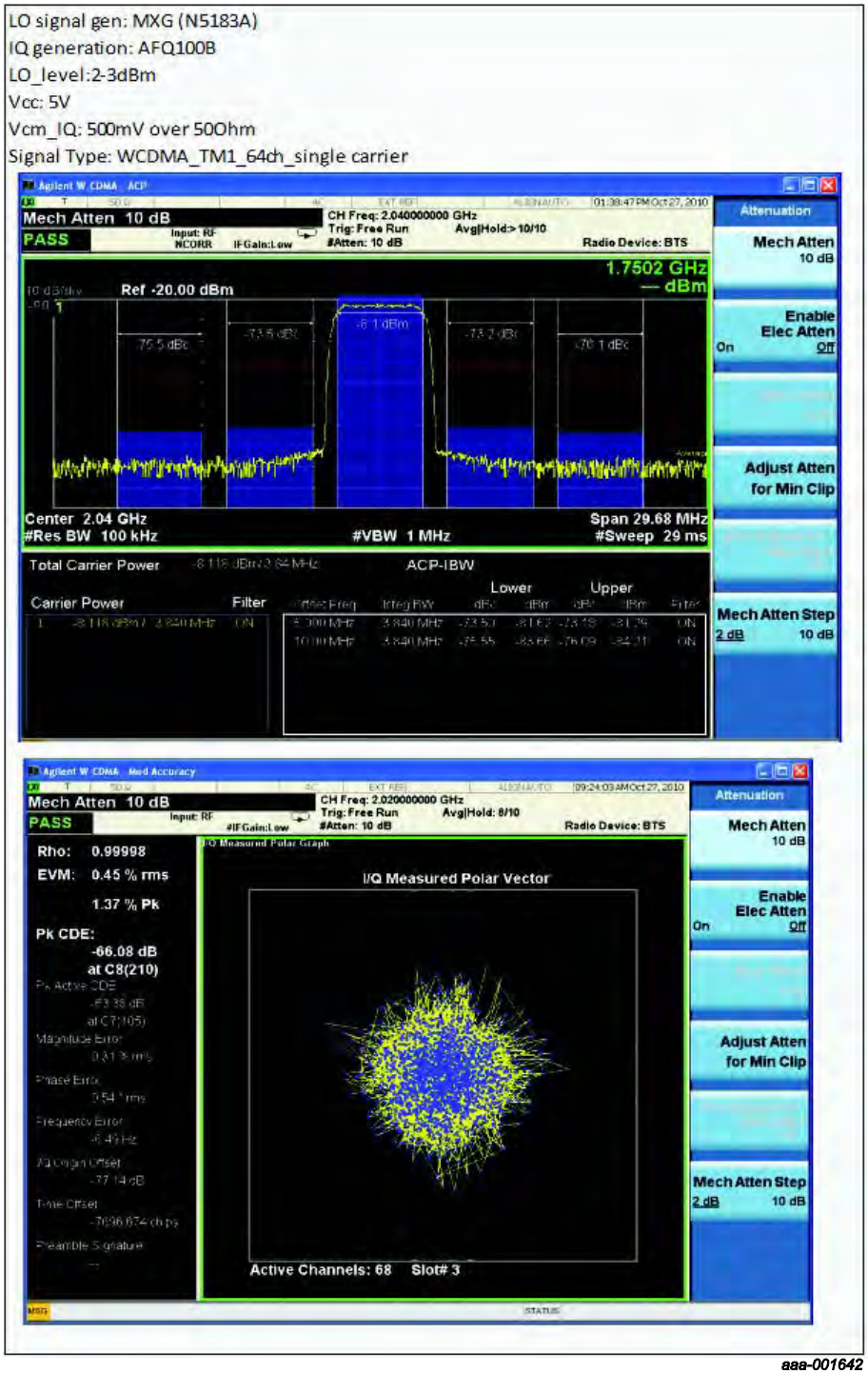
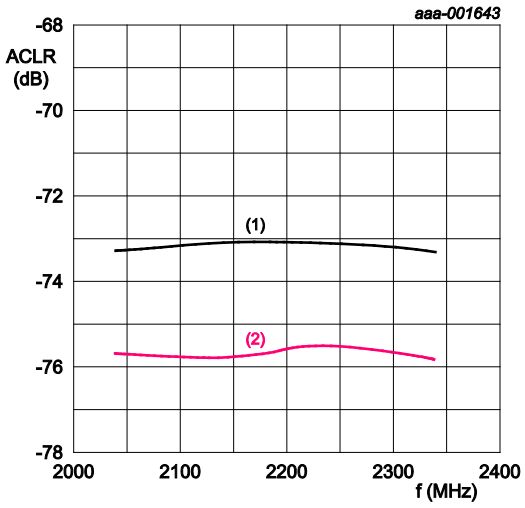


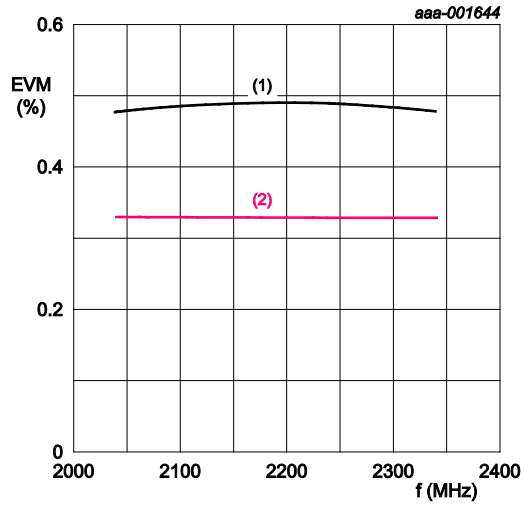
Fig 46. **One carrier WCDMA P_o = -8dBm**



(1) ACLR_5M; $P_{i(lo)}$ = 2 – 3 dBm; V_{CC} = 5 V; P_O = -8 dB.

(2) ACLR_10M; $P_{i(lo)}$ = 2 – 3 dBm; V_{CC} = 5 V; P_O = -8 dB.

Fig 47. **One carrier WCDMA - ACLR**



(1) $P_{i(lo)}$ = 2 – 3 dBm; V_{CC} = 5 V; P_O = -8 dB; PXA measurement.

(2) $P_{i(lo)}$ = 2 – 3 dBm; V_{CC} = 5 V; P_O = -8 dB; FSQ measurement.

Fig 48. **One carrier WCDMA - EVM**

6.3.5 Two carriers WCDMA

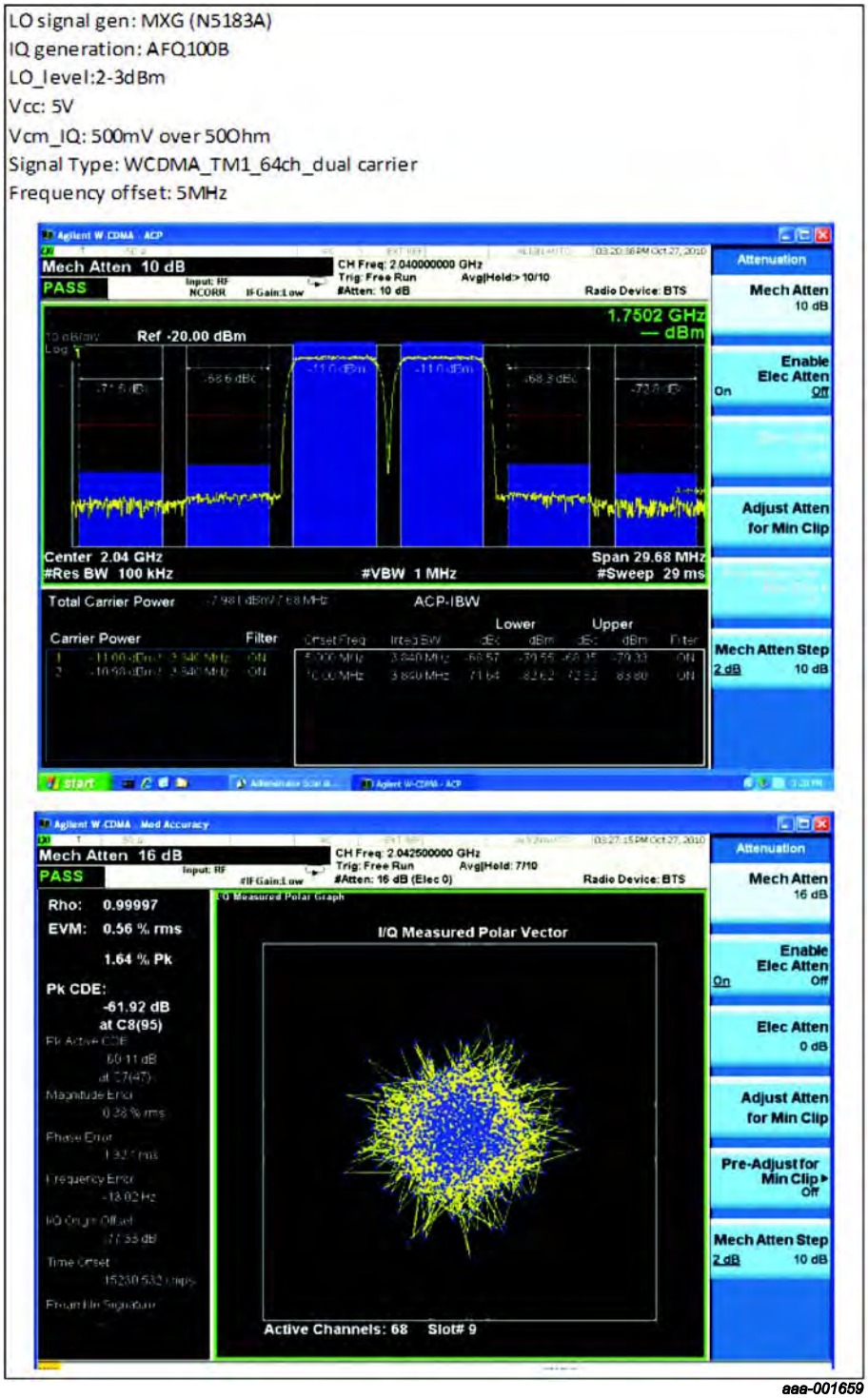
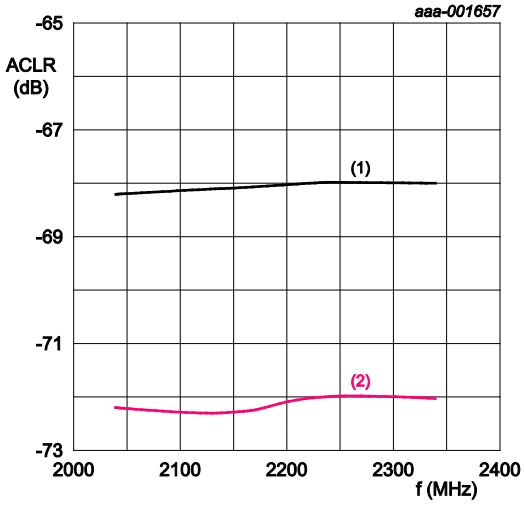


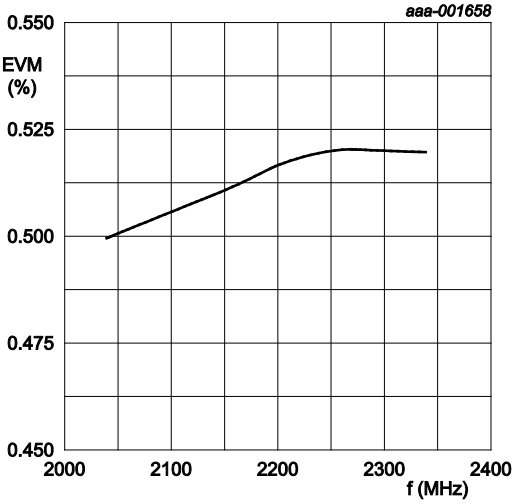
Fig 49. **Two carriers WCDMA**



(1) ACLR_5M; $P_{i(lo)}$ = 2 dB – 3 dB; V_{CC} = 5 V; P_o = -11 dBm per carrier.

(2) ACLR_10M; $P_{i(lo)}$ = 2 dB – 3 dB; V_{CC} = 5 V; P_o = -11 dBm per carrier.

Fig 50. **Two carriers WCDMA ACLR**



(1) $P_{i(lo)}$ = 2 dBm – 3 dBm; V_{CC} = 5 V; P_o = -11 dBm per carrier.

Fig 51. **Two carriers WCDMA EVM**

7. DC Interface between DAC1408D650 or DAC1627D1G25 and BGX7100

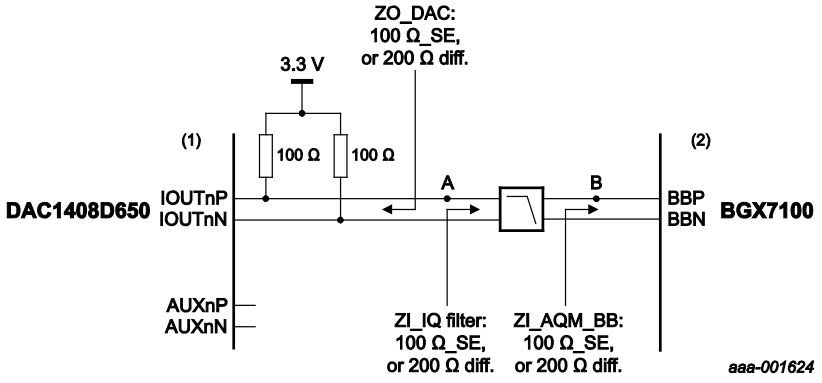
DAC1408D650/750 is a high speed 14-bit dual channel Digital-to-Analog Converter (DAC) with selectable 2x, 4x, 8x interpolating. Its serial interface “JESD204A” feature simplifies the baseband/FPGA to DAC interface and enables the high density integration, easy PCB layout, lower radiated noise and spurs, lower pin count, self-synchronous link, skew compensation. Because of its digital on-chip complex modulator, the

DAC1408D650/750 allows the complex pattern provided through lane0, lane1, lane2, lane3, to be converted from baseband to IF. The mixing frequency is adjusted via a Serial Peripheral Interface (SPI) with 32-bit Numerically Controlled Oscillator (NCO) and the phase is controlled by a 16-bit register. The Multiple Device Synchronization (MDS) guarantees a maximum skew of one output clock period between several DAC devices. MDS incorporates the modes Master/slave or All slave modes.

The DAC1627D1G25 is a 16-bit dual-channel digital-to-analog converter (DAC) with selectable 2x, 4x and 8x interpolating filters optimized for multi-carrier and broad band wireless transmitters at sample rates up to 1.25 Gsps. Supplied from 3.3 V and 1.8 V power sources, it integrates a differential scalable output current up to 31.8 mA. The mixer frequency is set by a high resolution 40-bit Numerically Controlled Oscillator (NCO). High resolution internal gain, phase and offset control provide outstanding image and LO rejection at the system analog modulator output. An inverse (sin x)/x function ensures controlled flatness at the DAC output. The LVDS DDR receiver interface allows a high data bandwidth (312.5 Msps) at the input.

When the system operation requires to keep the DC component of the complex spectrum which is the case for the zero-IF (direct up conversion) transmitters, the interface between DAC1408D650 or DAC1627D1G25 and BGX7100 must be DC coupled. In that case, the offset compensation for LO cancellation can be handled by making use of the digital offset control in the DAC without using AUXDAC outputs. However, if the complete dynamic range of the signal path of the DAC is preferred to be preserved only for the transmitted signal dynamic but not for the offset control, in that case the AUXDAC outputs are available for this purpose.

7.1 DC Interface without AUXDAC utilization

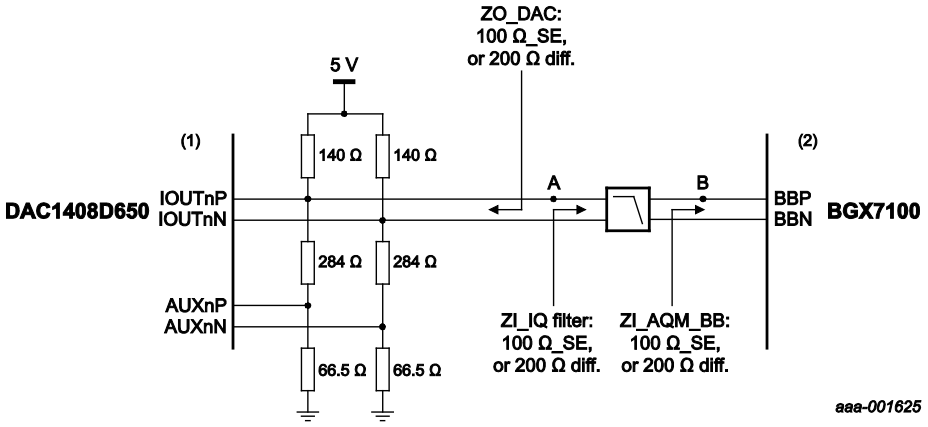


(1) IOUTnP/IOUTnN (with n = A or B); $V_{o(cm)}$ = 2.3 V; $V_{o(diff)(p-p)}$ = 1 V.

(1) BBP/BBN; $V_{i(cm)}$ = 2.3 V; $V_{o(diff)(p-p)}$ = 1 V; offset correction via signal path (IOUTnP/IOUTnN (with n = A or B)).

Fig 52. **Example of DC interface with $V_{i(cm)}$ of 2.3V**

7.2 DC Interface with AUXDAC utilization for DC offset compensation



(1) IOUTnP/IOUTnN (with n = A or B); $V_{o(cm)}$ = 2.59 V; $V_{o(diff)(p-p)}$ = 1 V.

(2) BBP/BBN; $V_{i(cm)}$ = 2.59 V; $V_{o(diff)(p-p)}$ = 1 V; offset correction up to 42 mV.

Fig 53. **Example of DC interface with $V_{i(cm)}$ of 2.59 V with DC offset compensation up to 42 mV via AUXDAC**

7.3 Recommendations about DC interface network:

In this chapter two different types of interface networks were proposed above as the examples. As well as the JESD204A serial interface feature of the DAC1408D650, the flexibility of the BGX7100 in terms of common mode I,Q input dc voltage levels (0.5 V ~3.3 V) and its finite input impedance (200 Ω) simplifies the complete transmit chain application and enables the further integration.

Depending on the preference to control the common mode dc offset, there are two different possibilities. The first possibility is to use the digital offset control in the DAC (through the signal/modulation chain) which needs only a pull-up resistor (100 Ω)) per DAC output (Fig.52). In that case, a small amount of DAC dynamic should be reserved for the offset control purpose. The second possibility is to use the AUXDAC outputs directly for differential offset control (LO cancellation) and combine these outputs with the DAC outputs in a proper way as proposed in Fig.53.

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